

A Low-Power, Low Data-Rate, Ultra-Wideband Receiver Architecture for Indoor Wireless Systems

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Abstract—In this paper, a novel architecture for a low data-rate, low-power consumption Impulse Radio (IR) Ultra-Wideband (UWB) receiver is presented. The received UWB signal is first downconverted to an intermediate frequency (IF). A criterion based on the average bit error rate (BER) will be used to optimize the IF. Using an IF instead of a downconversion to baseband removes the requirement to implement paths for the in-phase and the quadrature components and hence allow to reduce the power consumption. The signal at IF is converted to the digital domain by a set of 24 Redundant Signed Digit (RSD) Analog to Digital Converters (ADCs). The digitized signal is correlated with a predefined template and finally fed to the bit detector. The BER performance of the proposed receiver is evaluated using simulations in 802.15.3a multipath channels. Finally, the expected power consumption for the implementation of the receiver using a CMOS process is provided.

I. INTRODUCTION

UWB technology has attracted a lot of attention during last decade as a good candidate for short-range indoor communications [1], [2]. Different applications require different types of UWB receivers, depending on data rates, power consumption and implementation complexity.

A large number of different UWB receiver topologies have been reported in the literature. One of the most common receivers is the analog baseband correlation receiver [2]. While it performs well in ideal channels, this receiver has reduced performance in realistic multipath channels. Transmitted Reference (TR) receivers [3] and rake receivers [4] perform very well in multipath environments. Two different topologies of TR receivers can be found in literature. In [5], each pulse is differentially modulated with respect to the previous pulse, so each pulse is used as a reference and as a data pulse. On the other hand in [6], each transmitted pulse is replaced by two pulses, a reference pulse and data pulse. The reference pulse is delayed in the receiver to be correlated with the data pulse. The TR receivers capture all the multipath components of the received signal without any channel estimation, but on the other hand their very noisy correlation template results in degraded performance. Moreover, they need long accurate analog delay lines which are difficult to fabricate [7]. The rake receiver can collect all the received energy from the multipath components. However, the rake receiver requires a very complicated structure, with one despreader (correlator, rake finger) for each multipath component to be received. Another receiver topology is the fully digital receiver, which was introduced in [8]. In this architecture, the incoming pulses

are downconverted to baseband, and then sampled by two parallel ADCs and processed in the digital domain. This receiver requires high ADC speeds and hence high power consumption. Reducing the ADC resolution to one bit [9] avoids high speed ADCs and hence the power consumption is reduced, but at the cost of system performance degradations. In [10], matched filtering of the pulses with the pulse template is moved from the digital to the analog domain. In this case, the sampling frequency of the ADCs is reduced from Nyquist rate to pulse rate, and the ADC resolution is maintained the same. This receiver, having a more complex architecture than the common analog baseband receiver [2], also has limited channel compensation in the analog domain.

In this paper, we present a new receiver architecture where the pulse is downconverted to an IF frequency and directly converted by a set of 24 RSD ADCs to the digital domain where it is correlated with a predefined template. Therefore, there is no need for in-phase and quadrature paths and the ADCs can work at the pulse repetition rate so the power consumption can be significantly reduced.

This paper is organized as follows. Section II gives a description of our system including the transmitter, the channel model and the receiver. In section III, we evaluate the performance of the system through Monte Carlo simulations. The estimation of the power consumption of the analog part of our receiver is presented in section IV. Finally, conclusions are given in section V.

II. SYSTEM DESCRIPTION

In this section, we first discuss the choice of data and code modulation. Then, the channel model is presented, followed by a detailed description of the receiver architecture.

A. Signal and Modulation

Referring to previous theoretical analysis and numerical simulations [11], [12], it is noted that for the data modulation, Binary Phase Shift Keying (BPSK) outperforms Pulse Position Modulation (PPM) by 3 dB in AWGN when considering the BER performance. Therefore, we selected BPSK modulation for data transmission. For code modulation, BPSK was shown in [12] to provide approximately the same performance as 3 bit PPM (i.e., PPM with 8 modulation bins) in both AWGN and CM3 transmission channels for multiuser mitigation. As BPSK is already used for data modulation, its application to code modulation will not increase the transmitter or receiver

complexity and is thus selected. Hence, the transmitted waveform by the k th user can be expressed as

$$S^{(k)}(t) = \sqrt{E_g} \sum_{j=-\infty}^{+\infty} d_{\lfloor j/N_s \rfloor}^{(k)} b_j^{(k)} p(t - jT_f) \quad (1)$$

where $S^{(k)}(t)$ is modeling the transmitted signal by the k th user and $p(t)$ is a Gaussian pulse. The other parameters used in this model are the following:

- E_g is the energy transmitted for each pulse.
- N_s is defined as the number of pulses used to transmit one data bit. Hence, the bit energy is $E_b = N_s E_g$.
- T_f is the frame duration, i.e., the mean duration between two pulses. Therefore the bit duration is $T_b = N_s T_f$.
- $d_{\lfloor j/N_s \rfloor}^{(k)} \in \{-1, 1\}$ is the binary data sequence transmitted by the k th user.
- $b_j^{(k)}$ is the BPSK code. It produces a polarization of the pulse and can take the value -1 or 1 . The BPSK code is used to identify each transmitter.

At the transmitter the Gaussian pulse is up converted to $f_c = 6.5$ GHz such that the transmitted signal can be written as

$$f^{(k)}(t) = S^{(k)}(t) \cos(2\pi f_c t). \quad (2)$$

B. Channel Model

An accurate channel model is very important to obtain realistic simulations of the system performance. The IEEE 802.15.3a standard model is based on a modification of the Saleh-Valenzuela [13]. This model takes into account the clustering phenomena observed in several UWB channel measurements. According to [14], the channel impulse response can be described mathematically as

$$h_i(t) = X_i \sum_{l=0}^L \sum_{k=0}^K \alpha_{k,l}^i \delta(t - T_l^i - \tau_{k,l}^i) \quad (3)$$

where $\alpha_{k,l}^i$ are the multipath gain coefficients, T_l^i is the delay of the l^{th} cluster, $\tau_{k,l}^i$ is the delay of the k^{th} multipath component relative to the l^{th} cluster arrival time T_l^i , X_i represents the log-normal shadowing, and i refers to the i^{th} realization. In [14], four different measurement environments were defined, namely CM1, CM2, CM3 and CM4. In our simulations, we used the CM3 model as it provided the best fit with our real indoor channel measurements. We assume that N_u users are transmitting data asynchronously. User 1 is the user of interest and the other $N_u - 1$ users are considered as interfering users. The received signal can thus be modeled as

$$r(t) = f^{(1)}(t - \tau_1) * h^{(1)}(t) + \sum_{k=2}^{N_u} f^{(k)}(t - \tau_k) * h^{(k)}(t) + n(t) \quad (4)$$

where $*$ denotes the convolution operator, $\{\tau_k, k = 1, 2, \dots, N_u\}$ represents a time shift which accounts for user asynchronism, $\{h^{(k)}(t), k = 1, 2, \dots, N_u\}$ represents the k th user channel impulse response and $n(t)$ is the additive noise with two-sided power spectral density $N_0/2$.

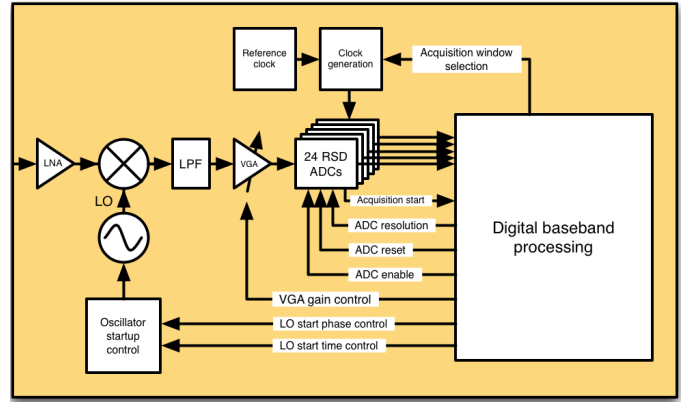


Fig. 1. Receiver Architecture

C. Receiver Architecture

The proposed receiver architecture, depicted in figure 1, is a heterodyne receiver as the received signal is downconverted to an intermediate frequency by mixing it with a local oscillator (LO) frequency f_{LO} . The resulting signal can be written as

$$g(t) = r(t) \cos(2\pi f_{LO} t + \phi) \quad (5)$$

where ϕ represents an arbitrary phase offset. The signal $g(t)$ is filtered, amplified, and converted to the digital domain. The baseband processing, such as the correlation with a predefined template is thus performed in the digital domain. Because of the intermediate frequency, there is no need for a frontend containing an in-phase and a quadrature path. By this mean, it is possible to reduce the total power consumption of the receiver. The analog to digital conversion is performed by a set of 24 RSDs, 6 bit ADCs, in a time interleaved mode. The time delay between two consecutive converters is 250 ps. Each converter operates at the pulse repetition rate. However, the equivalent sampling rate corresponds to 4 GS/s. This equivalent sampling rate is compliant with the Nyquist-Shannon sampling theorem. The 24 ADCs acquire the signal during an acquisition window with a maximum duration of 5.75 ns centered at the instant when a pulse from the user of interest is expected to arrive. Using a limited acquisition window instead of a continuous sampling allows an important reduction of the power consumption, but requires a more complex synchronization phase. The selection to use RSDs comes from their inherent ability to add the received voltages at the sampling time. Therefore, the analog combination of several pulses, which may be required to increase the signal to noise ratio (SNR), does not require any additional components. A simplified pulse template is proposed for the reception. In figure 2, it is compared to the received signal (without noise, and assuming an ideal channel) after the downconversion and the lowpass filter. The template is not a sine at the IF frequency, but a waveform closer to the second derivative of the Gaussian pulse. As the template does not match perfectly the signal, the receiver performance in AWGN will be lower than the one of a matched filter receiver. However, in a dense multipath channel, such as CM3, the proposed template provides an improved average performance compared to a template matched for an AWGN

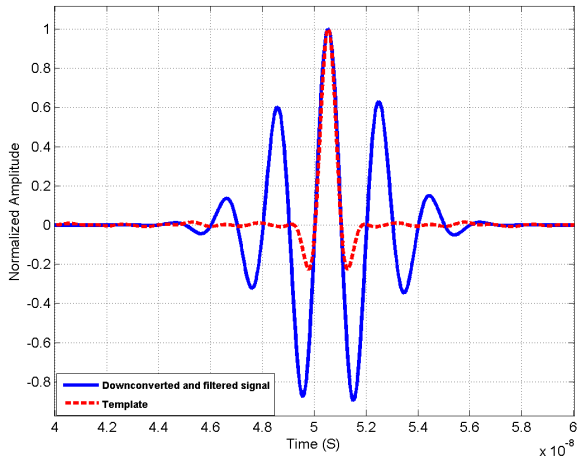


Fig. 2. Template and the received signal after downconversion to IF (500 MHz) and filtering with a lowpass filter of 1 GHz cutoff frequency

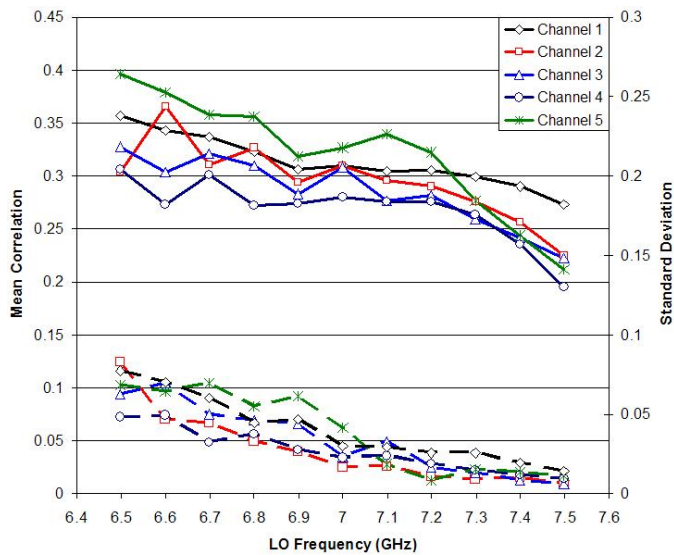


Fig. 3. Correlation value (solid) averaged for $\phi \in [0 \dots 2\pi[$ and the standard deviation (dashed) in relation to the LO frequency (For clarity, only the results for 5 channels are presented)

channel. The proposed template depends on the intermediate frequency, but is independent of the pulse duration. It may thus be considered as an alternative to a matched filter when the receiver is not able to accurately estimate the characteristics of the propagation channel.

Since the template depends on the intermediate frequency, the selection of the intermediate frequency will also influence the resulting performance. To estimate a promising intermediate frequency and its associated template, the correlation values between the local template and the received (noiseless) signal have been computed for many different realizations of the CM3 channels.

For each frequency of the LO the correlation between the received signal and the template was obtained for many different phase differences between the transmitted signal and the LO and then the mean value was calculated. To have an idea about

TABLE I
SET OF PARAMETERS USED FOR THE PERFORMANCE EVALUATION

Parameter	Value
Pulse shape $S(t)$	Gaussian
Pulse duration	2 ns
Center frequency at the emitter	6.5 GHz
Pulse repetition rate	10 MHz
Pulses per bit	16
Number of simultaneous users	10
LO frequency at the receiver	7 GHz
Low pass filter cut of frequency	1 GHz

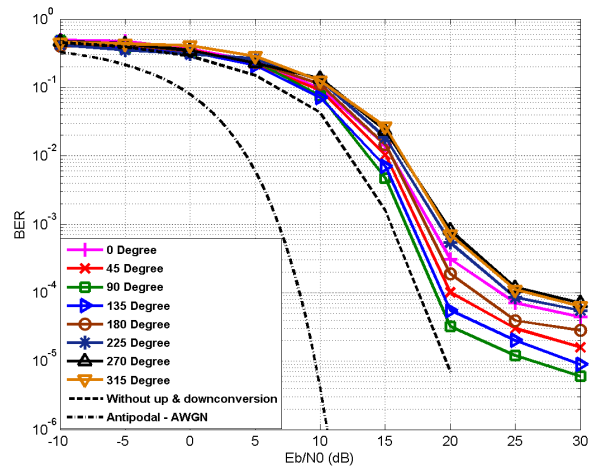


Fig. 4. BER in CM3 channel vs. E_b/N_0 for BPSK-BPSK UWB system with nine interfering users for $N_s = 16$.

the variation of the correlation as a function of the phase, the standard deviation was calculated for each LO frequency. From figure 3, we can see that the higher the LO frequency, the lower the correlation sensitivity (standard deviation) to the phase is. However, in the average, the correlation value decreases, and hence less energy is received. This decrease in the correlation value when the LO frequency increases is due to the cutoff frequency of the low pass filter. An optimum selection will hence select a compromise for the intermediate frequency. In the following, a LO of 7 GHz and low pass filter of 1 GHz cutoff frequency have been selected. The BER performance for this LO is considered in section III.

III. PERFORMANCE EVALUATION

To verify the functional behaviour of our receiver, the BER of the system was simulated in Matlab in the presence of multipath and nine interfering users. The simulations parameters are listed in Table I. During simulations each user is assigned a random channel and we assume that all the users transmit with the same amount of power. The multiuser codes for BPSK are chosen randomly. Using Monte Carlo simulation, the simulations were performed until at least 200 bit errors had been detected or when 1 Mbit had been transmitted. Figure 4 shows the BER simulations of our system for different phase difference between the transmitted pulse and the LO. The BER curve for the system in CM3 channel but without up

and downconversion of the pulse is also shown in figure 4. We notice that the reduction in power consumption by using one path instead of the in-phase and quadrature paths in the front end leads, at 10^{-3} BER, to a degradation between 1 and 4 dB depending on the phase differences between the transmitted signal and the LO. A value of 20 dB of E_b/N_0 is required to maintain a BER value of 10^{-3} regardless of the phase difference between the transmitted pulse and the LO. Comparing our simulation results to the theoretical antipodal BER in an AWGN channel we notice that for small values of E_b/N_0 the BER curves diverge from the AWGN case since the energy of only one of the multipath is captured. For large values of E_b/N_0 , the interference is dominating and the curves are showing saturation in BER performance.

IV. IMPLEMENTATION

An estimation of the power consumption of the proposed receiver architecture is presented in this section. This estimation is based on simulations made for each component. All simulations are made for UMC's RF CMOS 0.18 μm and a power supply voltage of 1.8 V.

The LNA is directly connected to the antenna. It has a gain of 13 dB with a frequency range from 5.5 GHz to 7.5 GHz and a noise figure of 4 dB. The power consumption of the LNA is estimated to be 4.3 mW. The LO is a three stage ring oscillator and its power consumption is estimated to be 14.4 mW. The mixer is a conventional double-balanced Gilbert mixer. It consumes 1.8 mW. The lowpass filter attenuates the $f_{\text{RF}} + f_{\text{LO}}$ component at 13.5 GHz, the 6.5 GHz LO feedthrough as well as the noise above 1 GHz. Due to its high cut-off frequency, this filter can be implemented using passive components directly on the chip and therefore its power consumption can be neglected. The power gain of the VGA is 45 dB, its power consumption is estimated to be 5 mW at 1.8 V. The ADC block consists of 24 RSDs, six-bit ADCs in a time interleaved mode. The power consumption of each ADC is estimated to be 63 μW which results in 1.5 mW when the 24 ADCs are enabled.

The overall power consumption of the analog part can be calculated as:

$$P_{\text{an}} = P_{\text{LNA}} + P_{\text{MIX}} + P_{\text{ADC}} + P_{\text{LO}} + P_{\text{VGA}} \approx 27 \text{ mW} \quad (6)$$

Based on low pulse duty cycling the power consumption of some components can be further reduced by turning them off. Based on our simulations, the start up time of the LO is 1 ns and since the acquisition window is 5.75 ns, the LO can be turned off during 93 % of the time, which means that the power consumption of the LO can be reduced to $14.4 \text{ mW} \cdot 7/100 = 1 \text{ mW}$. During the synchronisation phase, the 24 ADCs are required to be on, which is not the case during the tracking or data communication phase where only 9 ADCs have to be enabled. The other components have a start up time of 0.5 ns, hence we can turn them off during 94 % of the time, which means that the power consumption of these components can be reduced to $11.2 \text{ mW} \cdot 6/100 = 0.7 \text{ mW}$. The total power consumption after duty cycling, during the synchronization phase, is estimated to be 3.2 mW, while in the tracking phase the power consumption can be reduced to 2.3 mW.

V. CONCLUSION

A low-power, low data-rate IR receiver architecture has been proposed. The pulse is downconverted to an intermediate frequency of 500 MHz instead of baseband such that the quadrature path in the receiver frontend can be omitted. This allows an important reduction of the power consumption. The analog to digital conversion is performed by a set of 24 RSDs, 6 bit ADCs, which are working at the pulse repetition rate. This reduces further the power consumption. The resulting power consumption of this receiver at 10 MHz pulse repetition rate and 0.625 Mb/s data-rate was estimated to be below 2.5 mW when duty cycling is used. Monte Carlo simulations showed a performance degradation between 1 and 4 dB compared to a baseband communication system in CM3 channel.

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