

Research Letter

A Programmable Receiver for Communication Systems and Its Application to Impulse Radio

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The design of a programmable receiver for an ultra wideband (UWB) communication is presented. The receiver is using a fast analog to digital converter (ADC) and a field programmable gate array (FPGA) allowing a rapid performance evaluation for various system architectures and signal processing algorithms. To demonstrate the performance and the versatility of the receiver, a simple communication system and a localization system are implemented. The accuracy of the latter is presented for an indoor environment.

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1. Introduction

With the recent progresses in digital electronics, the concept of the software defined radio (SDR) has gained a lot of interest for rapid development and prototyping of communication systems. A versatile SDR for wideband signaling without an application specific analog front-end requires a high sampling rate. In consequence, the specifications for the ADC and the digital signal processing units are tight. The presented receiver uses an FPGA for the signal processing, because it provides a well-balanced ratio between its available processing power and its reconfigurability. Although platforms with an ADC and an FPGA are commercially available up to several gigasamples per second, we have developed a custom programmable receiver to fit our needs. Among others they include the availability of an accurate, tunable quartz clock, the option to synchronize several programmable receivers, and a convenient mean for the data exchange with a personal computer (PC). In Section 2, the hardware and the software of the platform is presented considering the example of a communication system. In Section 3, the versatility of the programmable receiver is demonstrated for an indoor localization system. Finally, some concluding remarks are given in Section 4.

2. Communication System

In this section, a noncoherent receiver for an impulse radio (IR) communication system is presented. A mathematical description of the IR is followed by a description of the hardware of the transmitter and the receiver. Then, the algorithms are presented. The communication system has a low complexity and applies to applications with a restricted data rate using a pulse delay modulation.

2.1. Signaling and Modulation. Impulse radio is one flavor of UWB and is based on the transmission of short-duration pulses $p(t)$. Among others, the information to be transmitted can be used to modulate the amplitude, the polarity, or a delay of the pulses. In the following, a time hopping (TH) signaling scheme is considered, where each transmitter is attributed an unambiguous spreading code $\{c_{k,u}\}$. The transmitters are numbered by u and the pulses by k with $0 \leq k < N_f$. The resulting signal for one user is illustrated in Figure 1. When no other information than the spreading code is transmitted, the generated signal $s_u(t)$ is given by

$$s_u(t) = \sum_{k=0}^{N_f-1} p(t - kt_f - c_{k,u}t_c), \quad (1)$$

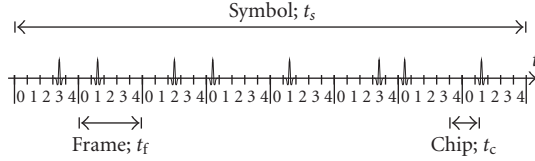


FIGURE 1: Transmitted signal for an impulse radio with a second derivative Gaussian pulse and code sequence $\{3, 1, 2, 0, 1, 3, 0, 1\}$.

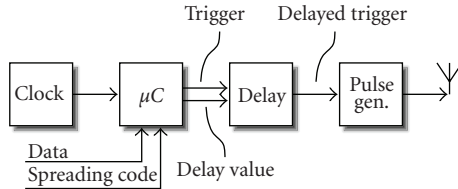


FIGURE 2: Transmitter block representation.

where t_f and t_c are the frame and the chip duration, respectively. From (1), it follows immediately that the transmission time of the k th pulse is

$$T_{k,u} = kt_f + c_{k,u}t_c, \quad (2)$$

and that the delay between the k th and $(k + 1)$ th pulse is

$$\Delta T_{k,u} = t_f + (c_{k+1,u} - c_{k,u})t_c. \quad (3)$$

It is noted that an extension to include pulse-position modulation (PPM) for which the transmitted information contains any additional data is straightforward.

2.2. Transmitter. To test the receiver, a transmitter including a baseband pulse generator has been built using standard electronic components. Figure 2 shows its block diagram. A microcontroller controls the delay generation and provides a trigger signal. By the means of a digital delay element, the trigger signal is delayed by the microcontroller according to the user's spreading code in steps of 2 nanoseconds before being fed to a pulse generator. The pulse generator is based on a bipolar transistor in avalanche mode. The generated pulse has approximately a Gaussian shape and covers a -10 dB bandwidth of about 750 MHz. The frame rate is 100 kPulses/s and the frame duration is approximately 10 microseconds. The number of pulses per symbol N_f is 16. The power density (before the transmitting antenna) is about -20 dBm/MHz when averaged over one symbol duration. For a location system for which the transmitter may send one symbol per second, the power density is -58 dBm/MHz when averaged over one second. A typical received and amplified pulse for a communication range of 7 m in an indoor propagation channel is illustrated in Figure 3.

2.3. Receiver. A block diagram of the receiver is shown in Figure 4. The received signal is captured using a wideband antenna. It is amplified by 18 dB and fed to a balun. The balanced signal is then converted into a stream of 8 bit

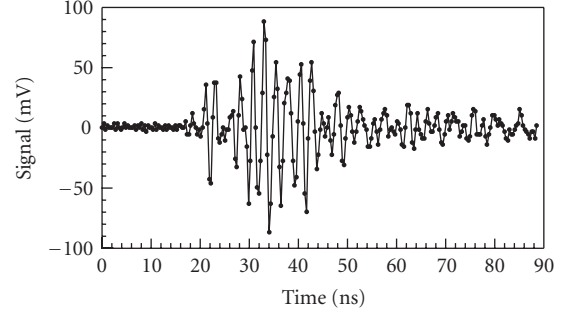


FIGURE 3: Typical representative of a received amplified pulse.

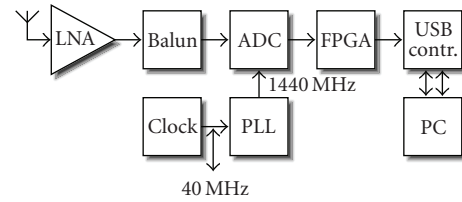


FIGURE 4: Receiver block representation.

digital values with a sampling rate of 2.88 GS/s (resulting in a data rate of 23.04 Gbit/s). The clock signal for the ADC at 1.44 GHz is generated from a 40 MHz reference clock using a phase-locked loop. At the output of the ADC, 4 sample values with 8 bit are provided in parallel. Each one of the 32 low-voltage differential signaling (LVDS) connection has a data rate of 720 Mbit/s. The FPGA is capable to acquire these streams of data, but cannot process them serially. At each input, a one-to-eight deserializer is placed. This results in 256 parallel signals with an update frequency of 90 MHz. They are reordered in the descrambler to an array containing the latest 32 samples represented as 8 bit values. This array can finally be processed in real time on the FPGA. An example of an implemented algorithm on the FPGA will be presented in Section 2.4. The outcomes of the signal processing on the FPGA can be transferred at a moderate data rate to a PC by the means of a universal serial bus (USB). This is convenient to implement parts of the processing algorithms on a PC.

2.4. Pulse TOA Measurement. As explained in Section 2.1, the transmitted information is contained in the delays of the pulses. In the following, a receiver is presented, that measures the pulse time of arrivals (TOAs) and sends these values to a PC for the remaining processing. To estimate the pulse TOAs, several algorithms have been proposed, for example [1, 2]. For simplicity, a threshold algorithm is used. Its working principle is illustrated in Figure 5. The FPGA compares the amplitude of the received signal with a threshold that can be selected by the software in the PC. When the signal exceeds the threshold, the instant t_k is stored. The resolution of the pulse TOA measurement is given by the sampling rate (347 picoseconds) and the accuracy depends on the propagation channel. To avoid to measure several pulse TOAs for a single pulse because of the multipath, the storage of pulse TOAs

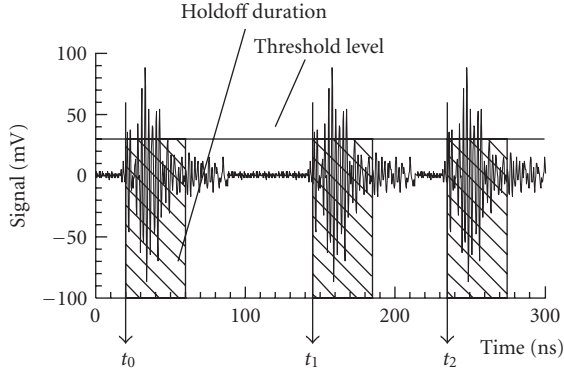


FIGURE 5: Illustration of the threshold detection algorithm to obtain the sequence $\{t_k\}$ (frame duration ≈ 100 nanoseconds selected for illustration only).

is disabled for a programmable hold off time after each acquisition.

2.5. Demodulation and Detection. For the demodulation and the detection of the transmitted information, for example, the identification of the transmitter based on the spreading sequence, the sequence of the pulse TOAs $\{t_k\}$ is compared to all the reference sequences $\{T_{k,u}\}$. To eliminate a constant delay for all the pulses in the sequence, one option is to compare the delays between two consecutive pulses $\{\Delta t_k\} = \{t_{k+1} - t_k\}$ with the reference sequences $\{\Delta T_{k,u}\} = \{T_{k+1,u} - T_{k,u}\}$ [3]. For a least squares algorithm, the detector selects the index u for which

$$C(u) = \sum_{k=0}^{N_f-2} (\Delta t_k - \Delta T_{k,u})^2 \quad (4)$$

is minimal. The principle can easily be extended if a data transmission is added to the identification of the transmitter in the reference sequences $\{T_{k,u}\}$. This demodulator does not require a synchronization between the transmitter and the receiver. It is particularly appropriate for applications, where the transmission time should remain as short as possible. For short-duration transmissions, a sufficiently low collision probability may be obtained even for a pure aloha protocol. The required calculation time for the least squares algorithm (4) increases linearly with the number of users u and the code length N_f . Such an approach may be suitable for a typical location estimation system where a limited number of tags should be identified. However, an extensive search over all possible code sequences is in general not possible. In such situations, the algorithm can be modified to lower the required calculation time, for example, by not searching for the entire code sequence at once, but by detecting the k th value of the code sequence individually based on the time difference Δt_k only.

3. Localization System

Proposed approaches to build a localization system include measurements of the signal strength, TOA, time difference

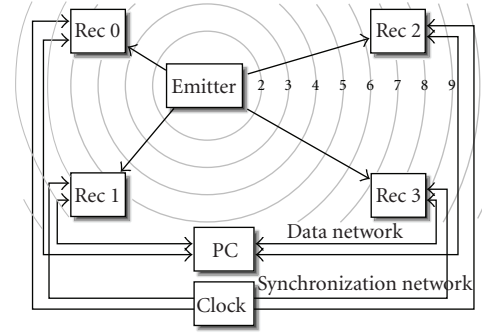


FIGURE 6: Architecture of a network-based localization system with synchronized receivers.

of arrival (TDOA), angle of arrival [4], or the propagation channel impulse response (location fingerprinting) [5]. In the following, the programmable receiver is used to build a localization system based on the measured pulse TOAs.

3.1. System Architecture. The selected architecture of the indoor localization system is shown in Figure 6. The tag to be located is equipped with a wideband transmitter. The signal is captured by four synchronized receivers placed in the laboratory at known positions. For a two-dimensional localization system, at least three receivers are mandatory. Two networks interconnect the receivers. The synchronization network provides a common reference clock signal to all receivers and hence eliminates drifts between the receiver's clocks. The measured TOAs are sent to the PC using the data network.

3.2. Signal TOA Estimation. It is assumed that the sequence of pulse TOAs $\{t_k\}$ is measured by the same means as described for the communication system in Section 2, that is, by measuring the instant at which the received signal exceeds a given threshold. To avoid any ambiguity, the sequence measured at the r th receiver is written as $\{t_{r,k}\}$. For the location estimation, a single TOA t_r per receiver is sufficient. In the following, a least squares method to estimate the signal TOA t_r from the N_f pulse TOAs $t_{r,k}$, $k = 0, \dots, N_f - 1$ is derived. A common delay t_r is searched, such that the sequence of the pulse TOAs $\{t_{r,k} - t_r\}$ becomes as close as possible to the reference sequence $\{T_{k,u}\}$. The least squares criterion is

$$t_r = \arg \min_{\delta} \sum_{k=0}^{N_f-1} [(t_{r,k} - \delta) - T_{k,u}]^2. \quad (5)$$

The signal TOA t_r can be obtained by setting the derivative of (5) with respect to δ to zero and is

$$t_r = \frac{1}{N_f} \sum_{k=0}^{N_f-1} t_{r,k} - \frac{1}{N_f} \sum_{k=0}^{N_f-1} T_{k,u}. \quad (6)$$

It is noted that the first sum is the arithmetic mean of the pulse TOAs of the pulses. The second sum is constant for all

receivers and hence has no impact on the location estimation. Therefore, it is convenient to define a compensated signal TOA t'_r as

$$t'_r = \frac{1}{N_f} \sum_{k=0}^{N_f-1} t_{r,k}. \quad (7)$$

The signal TOA t'_r does not depend on the transmission times $T_{k,u}$ and hence is independent from the transmitter identity.

3.3. Location Estimation. The positions $\vec{X}_r = (X_r, Y_r)$ of the receivers are assumed to be known and the location $\vec{x} = (x, y)$ of the transmitter should be estimated. For each receiver, pulse TOAs $t_{r,k}$ are measured with respect to the r th local clock of the receiver. From the pulse TOAs, the signal TOA t'_r is calculated for each receiver. We assume a delay δt_r between the local clock and the global clock. The global clock is a fictive clock, simplifying the equations for the synchronization and the location estimation. Because of the synchronization network, δt_r is a constant and does not vary over time. Let t_t be the transmission time of the signal measured using the global clock. The time of flights are given by

$$\begin{aligned} \text{TOF}_r &= (t'_r - \delta t_r) - t_t \\ &= c \|\vec{X}_r - \vec{x}\|, \end{aligned} \quad (8)$$

where $\|\cdot\|$ denotes the Euclidian norm and c is the propagation speed of the signal. The unknowns in (8) are estimated consecutively in two different modes. First, the delays δt_r are estimated in the calibration mode. Second, the location \vec{x} of the transmitter is calculated.

3.3.1. Calibration Mode. During the calibration mode, a transmitter is placed at a known position \vec{x} . To avoid error-prone handling, a reference transmitter may be mounted at a known fixed position. We assume $t_t = 0$ because a common delay for all receivers does not have an impact. Hence, (8) simplifies to

$$\delta t_r = c \|\vec{X}_r - \vec{x}\| - t'_r. \quad (9)$$

The approach described in (9) does not need any additional software for the calibration, as the functionality to measure the signal TOAs t'_r is already available. Furthermore, all relevant delays in the signal processing, for example, the propagation time of the clock signal, the propagation time of the signal from the antenna to the threshold detector in the FPGA, and the delays between the individual receivers are taken into account and automatically compensated.

3.3.2. Localization Mode. In the localization mode, (8) is solved for the location \vec{x} . The signal TOAs t'_k are measured and the preliminary estimated δt_r are subtracted. To solve (8), t_t can be considered as an additional unknown (set of spherical equations) or be eliminated by a pairwise subtraction of the equations (set of hyperbolic equations). When the system is overdetermined, the set of equations is

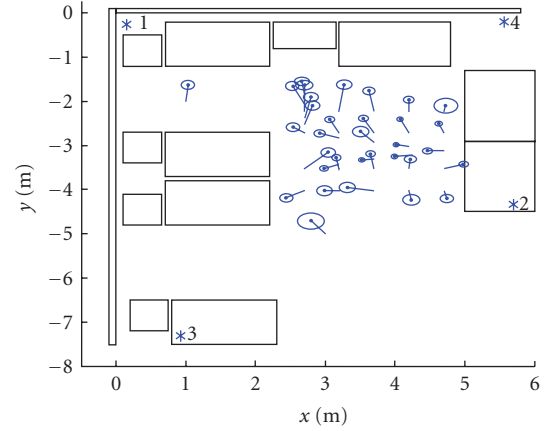


FIGURE 7: The outcomes of the location estimations when the transmitter is at selected positions. 65% of the outcomes are within the zones bounded by the circles. The connecting lines are relating the center of the circles, that is, the mean of the estimated locations, with the physical positions where the transmitter is placed.

solved using a least squares approach. Iterative methods, such as linearizing by a Taylor series expansion, and noniterative methods with comparable performance are common [6–8]. When one of the receivers provides inexact TOAs, the location estimation may be improved by eliminating the corresponding measurement and solving the nonoverdetermined set of equations. For the demonstrator, several sets with 4 and with 3 equations are solved using an iterative method. The final location estimation is taken as the median of the individual estimations.

3.4. Measurement Results. The localization system described in the previous sections has been implemented and installed in a laboratory at the University of Neuchâtel. Figure 7 shows a map of the room. The large rectangles represent bench tables with a shelf mounted on top of them to carry some electronic equipments. The four smaller rectangles at the left side of the map correspond to metallic drawer cabinets. The * mark the positions of the four receiving antennas. Throughout the room, 34 positions have been selected for testing the localization system. For reference, their coordinates were obtained by a measuring tape. The accuracy of these measurements is ± 1 cm, which is sufficient to evaluate the accuracy of the localization system. After power on, the system is calibrated by placing the transmitter at the reference position. The transmitter is then placed at the positions under test. The pulse TOAs are measured and transferred to a PC. The signal TOAs t_r are calculated and stored together with the delays δt_r in a file. This procedure is repeated at minimum 100 times for each position to obtain statistically significant results. The location estimations are calculated offline using the stored informations.

In addition to the map, Figure 7 also shows the outcomes of the localization system for selected positions. For each position, 65% of the outcomes are within the zone defined by the circles. The connecting lines are relating the center of the circles, that is, the mean of the estimated locations,

with the physical positions where the transmitter is placed. It is noted that the estimated locations have a bias compared to the physical position and that the statistical dispersion of the estimated locations is small. In the average, the bias is 31.9 cm and the circular error probability (CEP) is 7.4 cm. The error of the estimated locations is hence dominated by the bias, which results from a bias already present in the TOA measurements. It is due principally to an imperfect synchronization between the receivers and to a static error introduced by the threshold algorithm which may not always reliably detect the signal's direct propagation path from all the multipaths. To improve the location estimation by lowering the bias, a more accurate synchronization between the receivers and an improved algorithm for the pulse TOA estimation will be considered in the future.

4. Conclusion

In this paper, a programmable receiver based on an ADC and an FPGA is presented. It can be used for the development and the evaluation of communication systems covering a signal bandwidth of up to 1 GHz. Its versatility is demonstrated for an UWB impulse radio communication system and a localization system operated in an indoor environment. The latter is shown to have a CEP of 7.4 cm and a bias of 31.9 cm throughout a test room.

Acknowledgments

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Special Issue on Design, Implementation, and Evaluation of Wireless Sensor Network Systems

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